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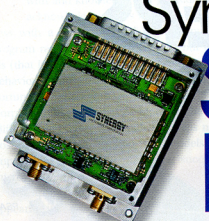


Synthesizers Shave Size And Noise

THESE SYNTHESIZERS ENLIST DDS TECHNOLOGY IN COMBINATION WITH A VCO TO ACHIEVE LOW PHASE NOISE AND EXCELLENT SPURIOUS PERFORMANCE—DOING SO AT A FRACTION OF THE SIZE AND COST OF CONVENTIONAL PLL SYNTHESIZERS.

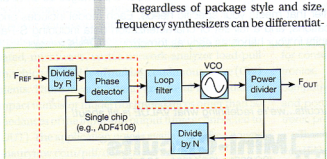
FREQUENCY SYNTHESIZERS are the essential signal sources for many high-frequency systems, from communications to test platforms. Synthesizers come in many forms, ranging from tiny system-on-a-chip (SoC) devices to large rack-mount units.[1–11] The number of technologies used to implement them is almost as diverse as their package styles, relying on analog methods, digital techniques, and sometimes a combination of the two approaches. For many applications, basic frequency synthesizer requirements call for a small unit with excellent spectral purity, but at an affordable price. These simple requirements drove the development of a new line of low-noise sources based on direct-digital synthesis (DDS) from Synergy Microwave Corp. (www.synergymwave.com)—one that comes at a fraction of the size and cost of currently available commercial sources.

Regardless of package style and size, frequency synthesizers can be differentiated by a number of key performance specifications. These include frequency tuning range (if not a fixed-frequency synthesizer), output power, output-power flatness across the tuning range, and a number of other parameters.[1] Acceptable levels for these parameters are usually set by the application of interest. Something like fast switching speed, for example, would be important in a frequency-agile communications system, but not as much as in other types of communications systems.[2]

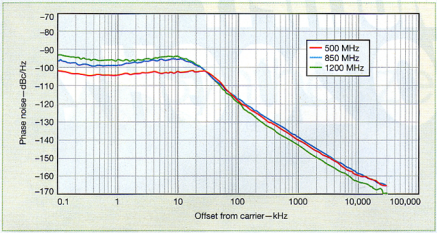
One of the more common types of synthesizer is a voltage-controlled oscillator (VCO) stabilized by a phase-locked loop (PLL). A conventional PLL-based frequency synthesizer includes a reference phase detector, loop filter, VCO, and VCO divider (**Fig. 1**).[3] Equation 1 defines the relationship between the output frequency, f_{out}, and reference frequency, f_{ref}[4]:

$$f_{out} = N \times (f_{ref}/R) \quad (1)$$

The phase-frequency detector (PFD) compares the two input signals f_{ref}/R and f_{out}/N and produces an error voltage proportional to the phase difference between them. The loop filter removes the high-frequency noise components from the PFD's output and limits the bandwidth of the error signal. The filtered error voltage is applied to the tuning port of the VCO to stabilize its resulting tuned frequency; the error signal drives the VCO frequency (f_{out}) so that the error voltage at the PFD output



1. This block diagram shows a simplified PLL synthesizer module.



2. This phase-noise plot typifies the performance of an integer-N PLL synthesizer.

is zero when locked.[5]

Typically, the VCO divider is implemented as a dual-modulus counter to obtain large continuous division of the VCO output. To vary synthesizer output frequency, f_{out}, N is changed. As Eq. 1 shows, the minimum output frequency step is f_{ref}/R. Operating the PFD at a lower frequency makes it possible to achieve a smaller step, but also increases R and N; in increasing N, the PFD noise also increases.[6] A PLL synthesizer's close-in phase noise is estimated by adding the noise of the synthesizer, PN_{SYN} to 20logN (where N is the divider value) and $10\log(f_{PFD})$:

$$PN_{TOT} = PN_{SYN} + 10\log(f_{PFD}) + 20\log N$$
$$= PN_{SYN} + 10\log(f_{REF}/R) + 20\log N \quad (2)$$

$$PN_{PD}\ (dBc/Hz) = PLL_{FOM} + 20\log_{10}(f_{VCO} - 10\log(f_{PD}))\ (frequencies\ are\ in\ Hz) \quad (3)$$

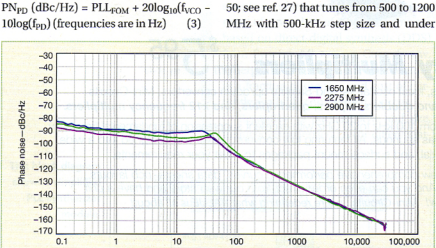
These simple equations reveal that PLL synthesizer design is a matter of tradeoffs.[7-41] As Eq. 2 shows, N should be low to minimize phase noise. But fine frequency resolution results from a PFD that is low in frequency, which leads to an increase in N and degraded noise performance. While loop filters can limit noise, they also prevent fast switching speed. A higher loop filter bandwidth yields faster switching speed, yet allows noise to pass. A narrower loop filter cuts the noise level, but with slower switching speed.

PLL frequency synthesizers can be implemented with integer or fractional values of N. **Figure 2** shows the typical phase noise characteristics of an integer-N frequency synthesizer (model FSW50120-50; see ref. 27) that tunes from 500 to 1200 MHz with 500-kHz step size and under 5-ms switching speed. The typical spurious noise is −65 dBc when operating with a 10-MHz reference frequency. To improve the performance of the integer-N frequency synthesizer, divider N can be implemented as a fractional divider rather than an integer divider.

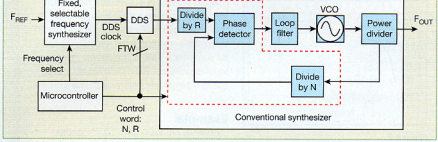
For example (as shown in **Fig. 3**), a commercial fractional-N source (model LFSW160290-50; see ref. 27), that tunes from 1600 to 2900 MHz in 500-kHz steps and works with a 10-MHz reference might have spurious levels of −60 dBc and switching speed of 1 ms. When better frequency resolution is needed, a DDS-based multiloop synthesizer design can be used, such as in **Fig. 4**. In this case, the DDS clock is fed by a selectable frequency synthesizer which provides a fixed set of frequencies based on the parallel selection lines. The DDS unit, with its resolution measured in microhertz, provides the fine frequency resolution. As with other frequency synthesizer designs, a DDS suffers tradeoffs, notably poor spectral purity and high spurious levels.

DDS spurious signal components that fall within the loop bandwidth are not attenuated by the loop filter. But they can be predicted and moved in frequency by using a different DDS clock frequency. With this approach, the PFD frequency of the output synthesizer can be high, improving phase-noise performance with a 10-MHz reference while still achieving 1-Hz frequency resolution. Such a design has switching speed of better than 1 ms with low phase noise and better than −70 dBc spurious performance from 1.1 to 2.5 GHz.

Figure 5 shows a typical block diagram for a DDS-based low-noise, fast-switching synthesizer based on a VCSO source. The typical synthesizer generates outputs ranging from 530 to 630 MHz with 1-MHz step size and spurious of −70 dBc or better. Since the analog phase detector has a low noise floor, the synthesizer bandwidth was kept large for faster switching time (about 200 µs) with low phase-noise performance. With recent developments in frequency synthesizers, the DDS shown in **Fig. 5** can be replaced with a single-chip flying-adder-based synthesizer.[5]



3. This phase-noise plot shows the typical performance of an fractional-N PLL synthesizer.



4. This block diagram shows a typical DDS-based dual-loop frequency synthesizer.

A design team at Synergy Microwave Corp., led by Dr. Dorin Calbaza, took on the challenge of developing a synthesizer that provided high performance in a compact size (3.25 x 2.25 x 1.25 in.) and could sell for low cost. The first consideration was to use an oscillator with octave tuning range of 4 to 8 GHz, as described in ref. 2. Octave tuning allows division by two, and frequencies above 4 GHz could be successively generated. Unfortunately, process, voltage, and temperature variations would make it difficult to guarantee frequency with precision any better than a few MHz. And synchronization techniques, such as locking the oscillator to a stable reference source such as an oven-controlled crystal oscillator (OCXO), would be needed for stabilization. As **Fig. 1** shows, a single-loop PLL can stabilize any frequency to the maximum oscillator's frequency.

In this approach, the low-noise crystal oscillator's frequency is multiplied by the PLL to the desired output frequency. Because of frequency multiplication, a 20 dB/decade degradation in phase noise is expected. For a 10-MHz crystal oscillator with phase noise of –174 dBc/Hz offset 10 kHz, the phase noise with multiplication at 8 GHz could not be better than –115 dBc/Hz. Taking advantage of PLL behavior, the PLL loop bandwidth would ideally be set to the frequency where the –115 dBc/Hz multiplied noise floor of the crystal intersects the trace of the noise produced by the oscillator—about 400 kHz for a typical scheme.[6] This is rather idealized, since the phase detector and the frequency dividers used in this PLL can degrade the crystal noise floor by about 20 to 30 dB in commercial PLL ICs.

The PLL contribution to the phase noise (PN_{PLL}) can be summarized as the root-mean-square addition of two components: PN_{PD}, a component determined by the phase detector comparison frequency, and $PN_{flicker}$, a flicker component independent of the phase detector comparison frequency given in Eqs. 1 and 2:

$$PN_{flicker}(dBc/Hz) = PLL_{flicker} + 20\log_{10}(f_{VCO} - 10\log_{10}(f_{Offset}) \quad (4)$$

In these equations, the PLL_{FOM} and $PLL_{flicker}$ are determined by the PLL design choices, and usually provided by the PLL manufacturer, where f_{VCO} is the output frequency of the oscillator, f_{PD} is the phase detector comparison frequency, and f_{Offset} is the frequency offset from the carrier used when estimating the phase noise. The noise added by the PLL circuit will then be:

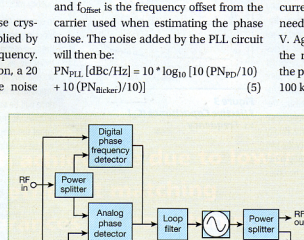
$$PN_{PLL}[dBc/Hz] = 10 * \log_{10}[10(PN_{PD}/10) + 10(PN_{flicker})/10)] \quad (5)$$

A typical case with $PLL_{FOM} = -220$, $PLL_{flicker} = -250$, $f_{VCO} = 8$ GHz, $f_{PD} = 10$ MHz, and $f_{Offset} = 10$ kHz will result in $PN_{PD} = -220 + 198 - 70 = -92$; $PN_{flicker} = -250 + 198 - 40 = -92$, and the resulting $PN_{PLL} = -89$ dBc. This is 26 dB higher than the –115 dBc/Hz contributed by the crystal oscillator considered above. For this circuit, setting the PLL bandwidth to about 20 kHz will result in the best phase-noise performance for any offset frequency. For an integer PLL, where frequency division is limited to integer numbers, the output frequency could only be set in 10-MHz increments.

This is a serious limitation, since many applications require a smaller step size, say 1 Hz to 10 kHz. For an ideal noise floor of –174 dBc/Hz with a 1-kHz comparison frequency, at 8 GHz that noise multiplied results in a –36 dBc/Hz PLL noise floor. Even if such noise would be acceptable, the PLL loop bandwidth should be set to about 100 Hz, subjecting the design to high level microphonics effects. Such a small loop bandwidth will also greatly increase the settling time of the PLL.

Settling time is determined by loop bandwidth and the time needed to charge the loop filter's capacitors with limited charge pump current. A design with a 10-kHz loop bandwidth may use a 1-µF capacitor in the loop. With a charge pump current of 5 mA, approximately 5 ms is needed to charge a 1-µF capacitor to 25 V. Again, with a 10-kHz loop bandwidth, the minimum comparison frequency at the phase detector's input would be about 100 kHz, limiting the step size to the same 100 kHz. This comparison frequency will ideally result in an 8-GHz output having a loop noise floor of –76 dBc/Hz when using a crystal oscillator with –174 dBc noise floor.

A fractional-N PLL helps overcome some of these limitations, dynamically changing the feedback ratio. As a result, the average divide ratio becomes a fractional number. The major advantage of this technique is that the phase-detector comparison frequency does not change with step size.



5. This is a block diagram of a typical fast-switching DDS-based frequency synthesizer.

In the following example, the output frequency is 7999.9 MHz and the reference requency is 10 MHz. The feedback divider divides 99 times out of 100 by 800 and divides 1 out of 100 times by 799. The average division ratio is 799.9, the output frequency is 7999.9 MHz and the phase detector comparison frequency is 10 MHz. The PLL phase noise is PN_{PLL} = –89 dBc/Hz, as calculated above, a major advantage over an integer PLL which ideally would only give –76 dBc/Hz.

The drawback of this technique is the introduction of the fractional spurious product in the spectrum that has a repetition rate determined by the period needed to average the divide ratio, f_{spur} = 100 kHz in the simple case presented above. Complex fractional-N PLLs will use higher-order DS modulation techniques to mitigate the spurious amplitude, while adding subfractional spurious content to the signal. Generally, a –40 to –60 dBc spurious amplitude is to be expected with this approach, and the PLL loop filter bandwidth must be reduced to attenuate the spurious content to an acceptable level. A PLL bandwidth of 10 kHz will impose a practical limit of about 100 kHz on the step size.

Spurious generated by the fractional-N PLL is caused by the inability of digital frequency dividers to position the transitions of the feedback clock with absolute accuracy in time. The time resolution of the transition is equal with the period of the clock provided at the divider's input. A DDS can overcome this limitation by adding a level of analog control to the transition. By generating an analog sinusoidal wave, the position of the zero-crossings of the sine wave can be controlled with high accuracy, resulting in close-to-carrier spurious levels at –100 dBc/Hz. It is worth mentioning that the DDS, or any fractional frequency divider, will exhibit a high spurious case when the input frequency of the DDS is close to a rational multiple of the output frequency. This spurious is called "integer boundary spur" and is particularly difficult to eliminate.

For frequency synthesis purposes, the DDS circuit could be considered as a low-noise frequency divider. The output frequency of this DDS divider is described by:

$$f_{DDS} = (N/2^k)f_{Clk} \quad (6)$$

where:

f_{DDS} = the DDS output frequency;

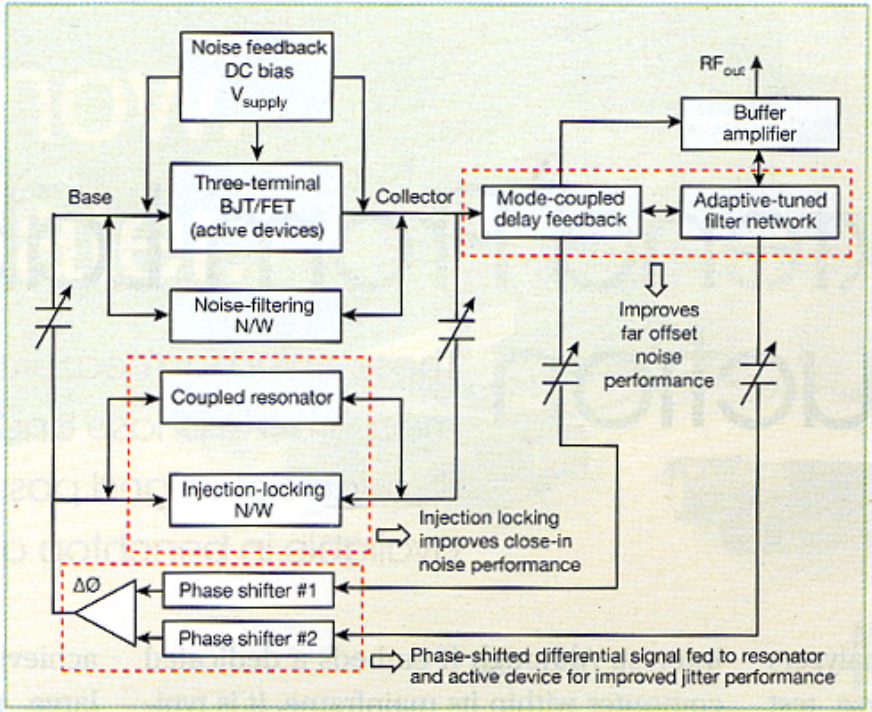
N = a digital number represented with k-bit resolution; and

f_{Clk} = the frequency of the DDS's input clock.

In practice, f_{Clk} is limited to $0.4f_{Clk}$, or about 400 to 1000 MHz, when using modern DDS ICs with f_{Clk} as large as 1 to 2.5 GHz. The resolution of the output frequency is typically set to 32 or 48 b.

The availability of low-cost, low-noise VCOs [27] clears the way for small, low-noise synthesizers. Part of using these sources

involves modeling surface-acoustic-wave (SAW) resonators under large-signal drive conditions for better insights about noise dynamics of close-in phase noise; then, manufacturable methods for producing high-purity and temperature-stable oscillators in chip form can be developed. **Figure 6** is a block diagram for a configurable user-defined multi-band low-noise VCO with 2-to-4-GHz/4-to-8-GHz/5-to-10-GHz/6-to-12-GHz tuning range. It is compact (0.3 x 0.3 x 0.08 in.), operates at 12 mA and 5 V, and exhibits phase noise of typically –135 dBc/Hz offset 1 MHz from the carrier frequency 2 GHz.[27] The DDS-based model KMTS2500-200800 synthesizer using high-performance adaptive dynamic mode-coupled, low-phase-noise VCO using



6. This is a block diagram of a typical low-noise, wideband VCO measuring 0.3 x 0.3 in. (See ref. 27.)

patented techniques.[13-26]

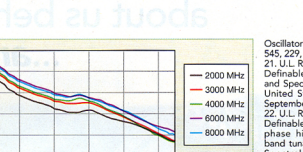
A low-noise PLL multiplies a reference frequency to the maximum frequency allowed by the DDS circuit. The DDS output signal is then filtered and provided as a reference to a secondary PLL that will multiply the frequency to the desired range. Depending on design choices, the phase-noise performance may be limited by the primary PLL, the DDS circuit, or the secondary PLL. However, the spurious performance is determined by the frequency multiplication and division implemented by the PLL circuits and the DDS.

With this module, it is desired to generate 2000.001 MHz using a 10-MHz reference. The low-noise PLL multiplies the 10-MHz clock to 1 GHz, and the DDS uses this signal to produce the 62.50003125 MHz required by the secondary PLL. Strong integer boundary spurious products may be noticed at this point in

(continued on p. 154)

the DDS output at 500 Hz offset from the ~62.5-MHz carrier. That 500-Hz spurious product will be amplified by 30 dB and would be practically impossible to filter out from the 2.000001-GHz output signal. The KMTS2500-200800-10 employs a proprietary algorithm that selects the best combination of divide ratios, avoiding spurious conditions.

The compact synthesizer module can generate 2-to-8-GHz outputs with a typical phase noise of –97 dBc/Hz offset 10 kHz from the carrier, and typical spurious performance of –50 dBc. **Figure 7** shows the typical phase-noise performance of the synthesizer for 2-, 4-, 6-, and 8-GHz outputs. The topology can be used at standard and custom frequencies for X and Ka band applications using low noise VCO,[27] saving the complexity and the compromised reliability of other reference source solutions. Finally, the **table** offers a summary of these results. MWRF



7. These plots show the phase noise of the DDS-based model KMTS2500-200800-10 synthesizer at four different carrier frequencies.

Summarizing the KMTS2500–200800's phase noise.

	Output frequency (GHz)				
	2	3	4	6	8
Offset from the carrier (kHz)	Phase noise (dBc/Hz)				
0.1	–89.88	–83.64	–81.56	–76.32	–77.42
1	–111.52	–104.51	–102.73	–97.01	–98.70
10	–123.82	–116.66	–114.90	–109.51	–111.04
100	–127.35	–119.99	–117.16	–114.05	–113.66
1000	–137.05	–133.81	–131.95	–127.50	–126.04
10,000	–153.82	–153.78	–151.36	–145.79	–144.16

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