



# Ultra-Low Noise Dielectric Resonator Oscillator

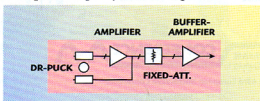
When high data-rates have to be transferred, as with M-QAM modulation in LTE, LMDS, fixed frequency point-to-point digital radio and satellite-links, these systems need low phase noise signal sources either free running or phase-locked. RADAR systems and Research Laboratories also require ultra-low noise sources to generate ultra-low noise carrier signals.

A wide range of military, industrial, medical, test and measurement markets demand these very stable frequency sources with enhanced phase noise performance and low thermal drift. A popular solution in the range of 3 to 18 GHz frequency spectrum is the dielectric resonator oscillator (DRO), recognized for its superiority in ultimate noise floor and spectrum purity when compared to other

competing solutions such as multiplied lower frequency fundamental sources.

Synergy Microwave is introducing a new generation of small, ultra low noise DROs to address these market needs. The free running CDRO1000-S from SMC has mechanical and electrical frequency tuning designed to give the best phase-noise performance for a 10 GHz DRO to serve these markets.

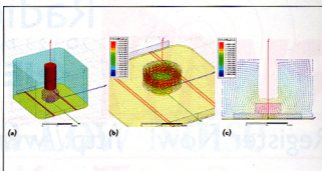
The circuit in **Figure 1** shows a typical block diagram of the DRO. The design challenge was to develop the lowest phase noise DRO, while minimizing costs through highly repeatable production builds. Such consistency in design and manufacturing could only be achieved through solid circuit simulation, by employing the latest state-of-the-art CAE tools such as ANSYS HFSS and Agilent-EEsof ADS/Momentum. The complete DRO design has been exercised and optimized using circuit and EM co-simulation (see **Figure 2**). This approach enabled us to achieve a high loaded figure of merit ( $Q_L$ ) for the dielectric resonator arrange-



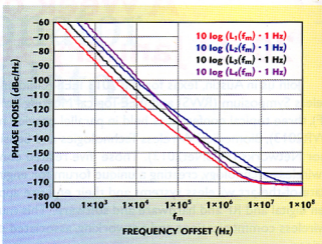
▲ Fig. 1 DRO block diagram.

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▲ Fig. 2 Four-port dielectrical resonator model (a), E-Field vector plot within the DR at resonance (b) and H-Field vector plot in YZ-plane (c).



▲ Fig. 3 The impact of possible impairments on the phase noise performance.

ment in conjunction with the oscillator core which is one of the preconditions for achieving lowest phase noise. The oscillator's main active device has been selected carefully with respect to noise figure and flicker noise, with optimum bias level conditions.

**Figure 3** illustrates the impact of possible impairments on the phase noise performance. The red trace identifies the measured phase noise performance of Synergy's new 10 GHz model number CDRO1000-8. The blue trace corresponds to a lower  $Q_L$  with identical oscillator core noise properties. The black and magenta traces correspond to identical  $Q_L$  but significantly higher effective noise figure or flicker corner frequency when the active device is not selected or biased optimally. A combination of these impairments together with nonlinear noise effects account for the much higher phase noise performance found in many competing DRO designs.

The CDRO1000-8 has a typical noise floor of -166 dBc/Hz which approaches state of the art performance. The measured phase noise reaches -111 dBc/Hz at 10 kHz offset as indicated in **Figure 4**. Mechanical and electrical tuning are available for frequency adjustment and phase locking. The frequency is factory set to 10 GHz and can be mechanically varied by approximately  $\pm 50$  MHz. The electrical tuning port varies the center frequency by  $\pm 1$  MHz with a tuning voltage of 1 to 15 V DC to compensate for frequency drift in phase locked

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systems. The temperature stability is typically specified at 80 ppm.

The oscillator supply voltage can vary between +7 to +10 V and the internal voltage regulation gives high immunity to power supply noise. The

supply-current is typically 50 mA and the temperature range is specified from  $-25^{\circ}$  to  $+70^{\circ}$ C. The output-power exceeds +8 dBm. The actual package size is approximately  $3.1'' \times 1.34'' \times 0.788''$ , including mounting flaps.

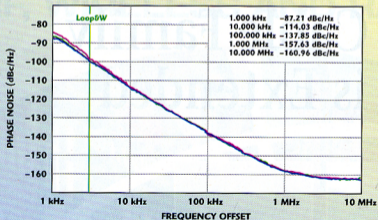
Similar to crystal oscillators, DROs tend to be prone to vibrational noise since the dielectric resonator itself cannot be secured mechanically. Therefore vibrations must effectively be damped by other means before they reach the dielectric resonator. The CDRO1000-8 is designed with rugged construction to minimize vibration noise and microphonic effects to prevent unwanted modulation.

Its excellent phase noise performance makes this DRO well suited for low-jitter communication systems, reference oscillators for phase noise measurement, RADAR systems, SDH/SONET, cable TV, SATCOM systems, aeronautical equipment, digital radios (QAM) and laboratory frequency references. Custom frequencies and packages (hermetic) can be developed on request.

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Settings		R&S FSUP 26 Signal Source Analyzer		LOCKED	
Signal Frequency:	10.000370 GHz	Residual Noise (T2 w/o spurs)	Int PHN (1.0 k.. 10.0 M)	-58.7 dBc	Phase Detector +0 dB
Signal Level:	8.79 dBm	Residual PM		94.624 m°	
Cross Corr Mode:	Harmonic 1	Residual FM		215.169 Hz	
Internal Ref Tuned:	Internal Phase Det	RMS Jitter		0.0263 ps	



▲ Fig. 4 Measured phase noise of CDRO1000-8.